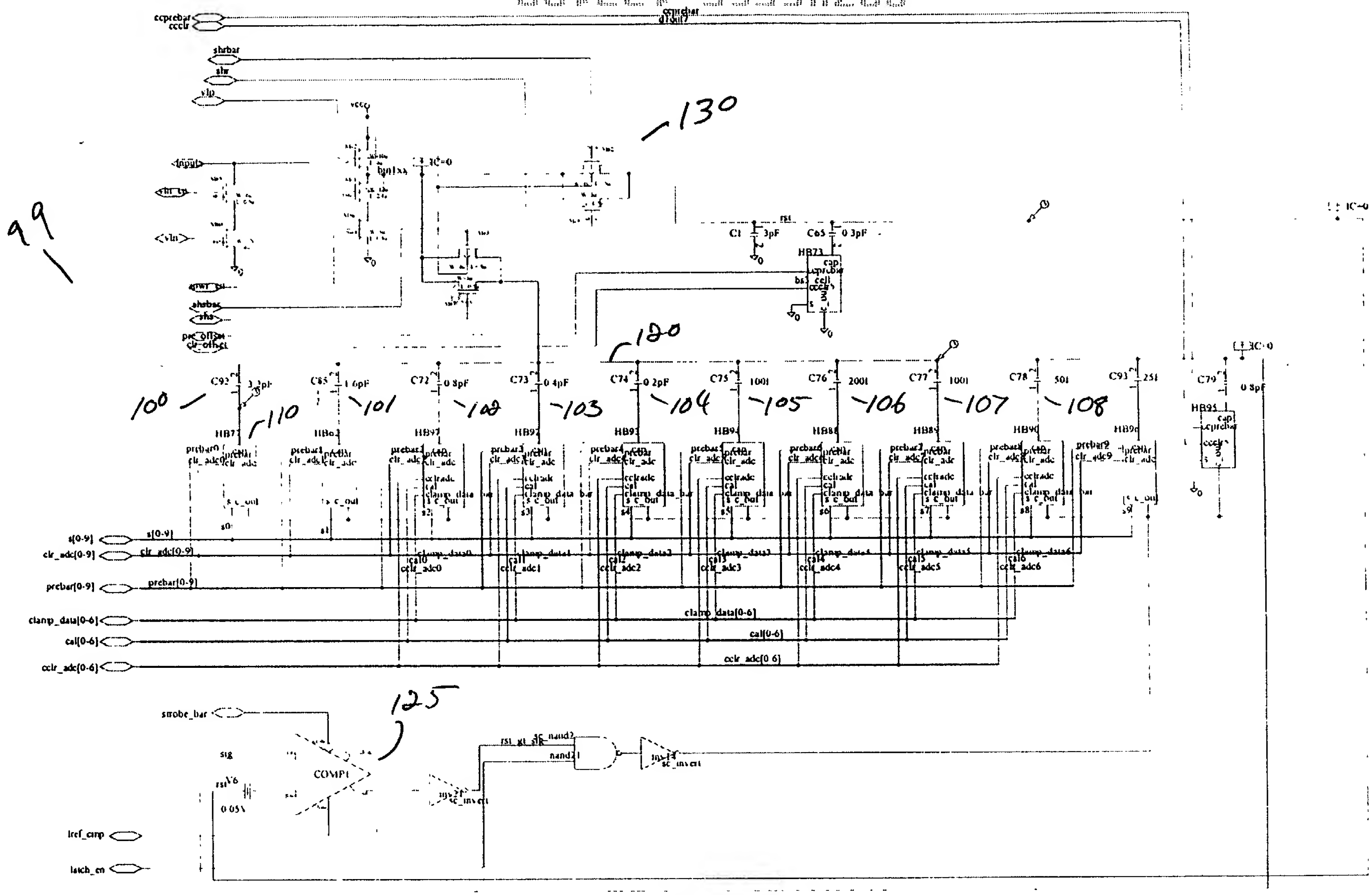

Fig. 1

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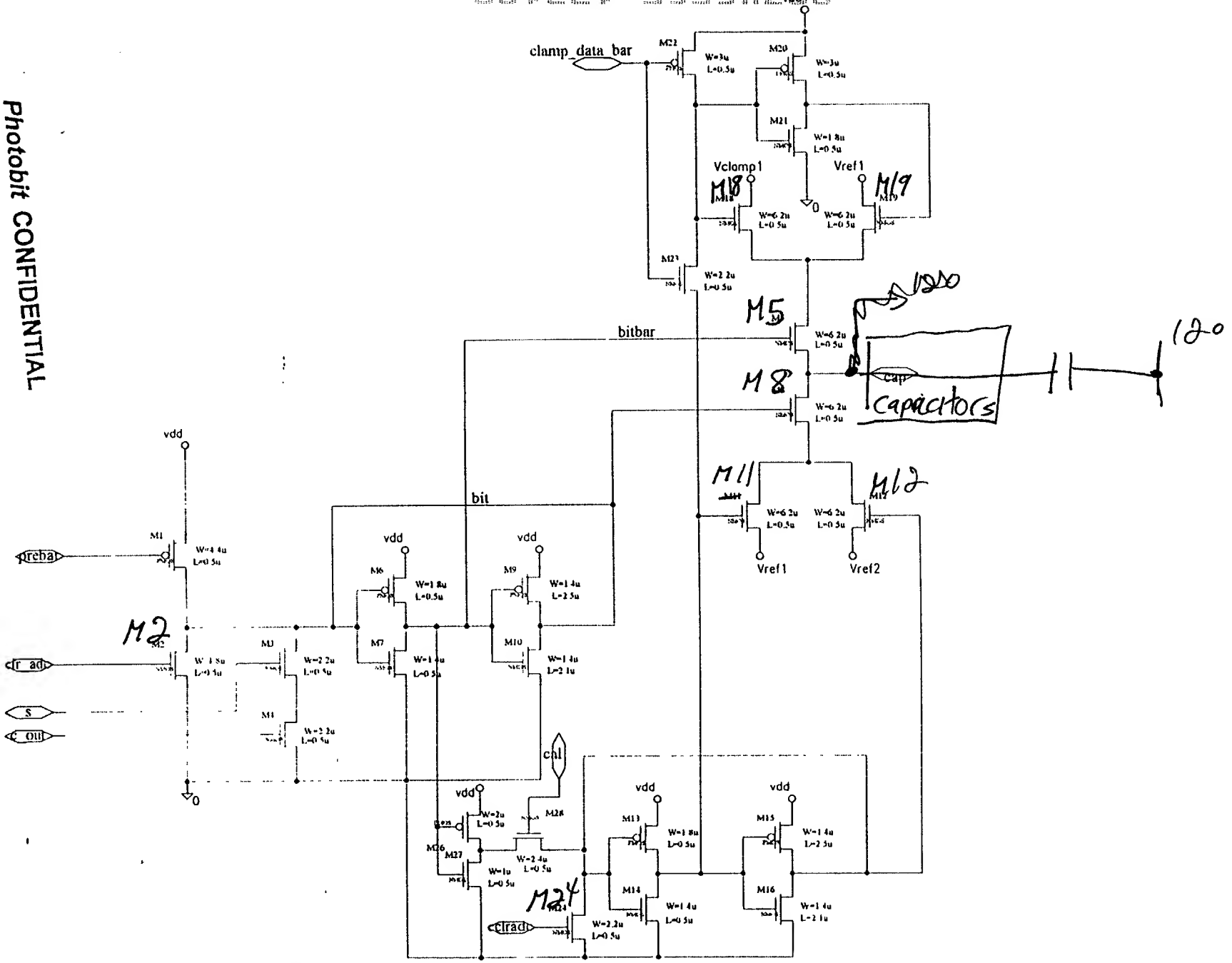

Fig. 2

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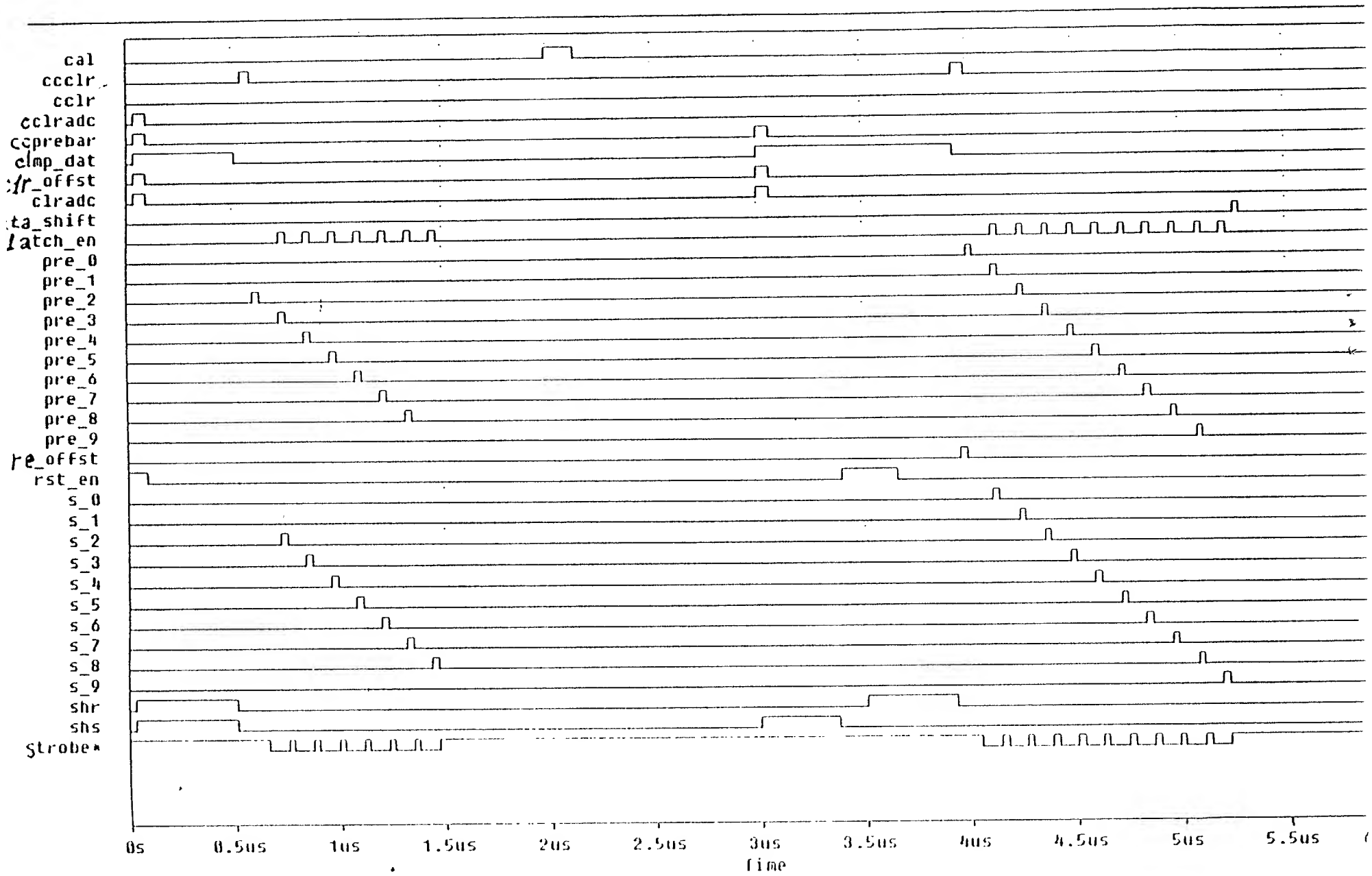
cal
ccclr
cclr
cclradc
ccprebar
clmp_dat
clr_offst
clradc
data_shift
latch_en
pre_0
pre_1
pre_2
pre_3
pre_4
pre_5
pre_6
pre_7
pre_8
pre_9
pre_offst
rst_en
s_0
s_1
s_2
s_3
s_4
s_5
s_6
s_7
s_8
s_9
shr
shs
Strobe*
0s
0.5us
1us
1.5us
2us
2.5us
3us
3.5us
4us
4.5us
5us
5.5us
Time

Fig.3

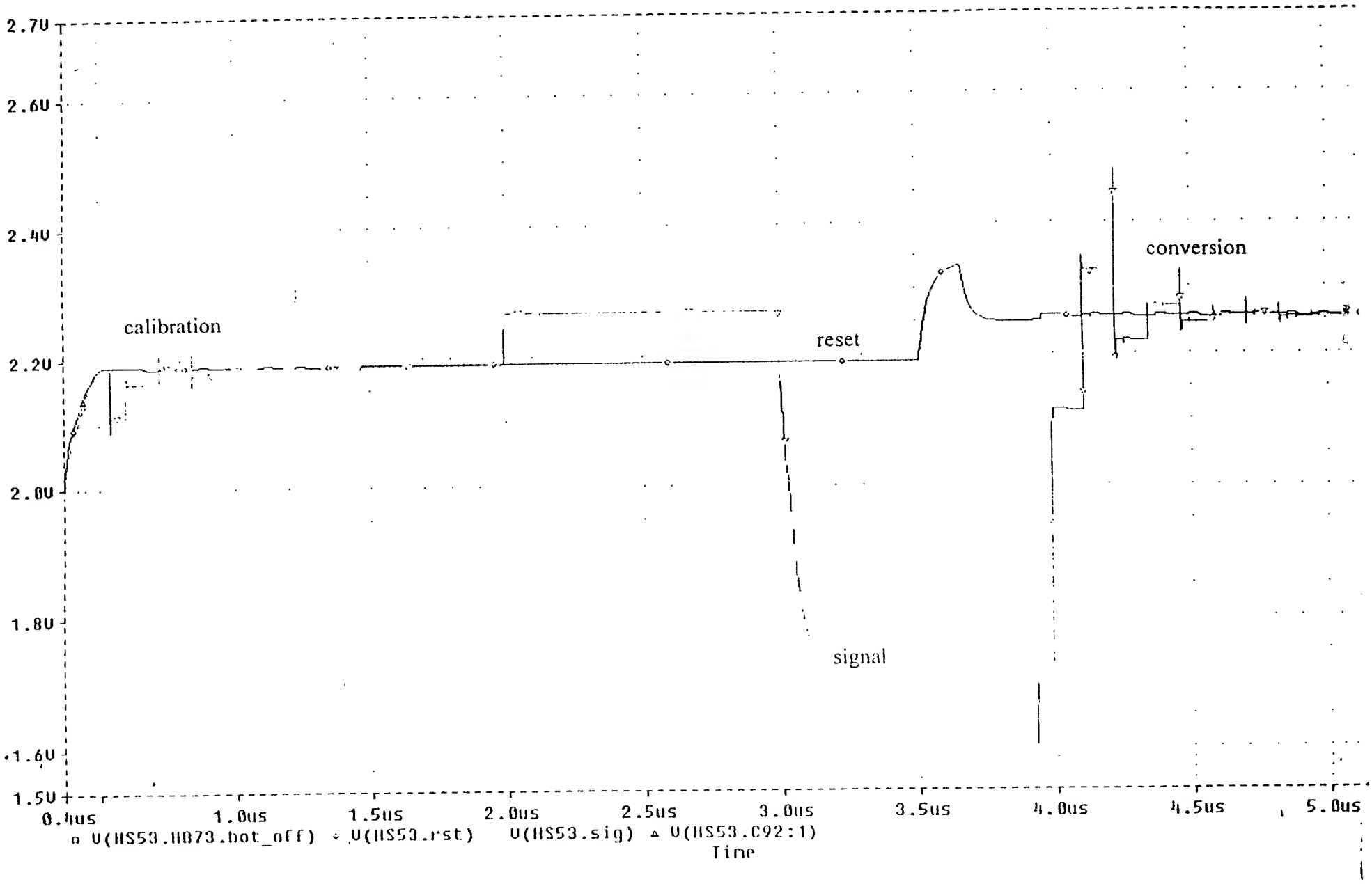
2.7U
2.6U
2.4U
2.2U
2.0U
1.8U
1.6U
1.5U
calibration
reset
signal
conversion
0.4us
1.0us
1.5us
2.0us
2.5us
3.0us
3.5us
4.0us
4.5us
5.0us
V(HS53.HB73.hot_off)
V(HS53.rst)
V(HS53.sig)
V(HS53.C92:1)
Time

Fig. 4

09746595.122100

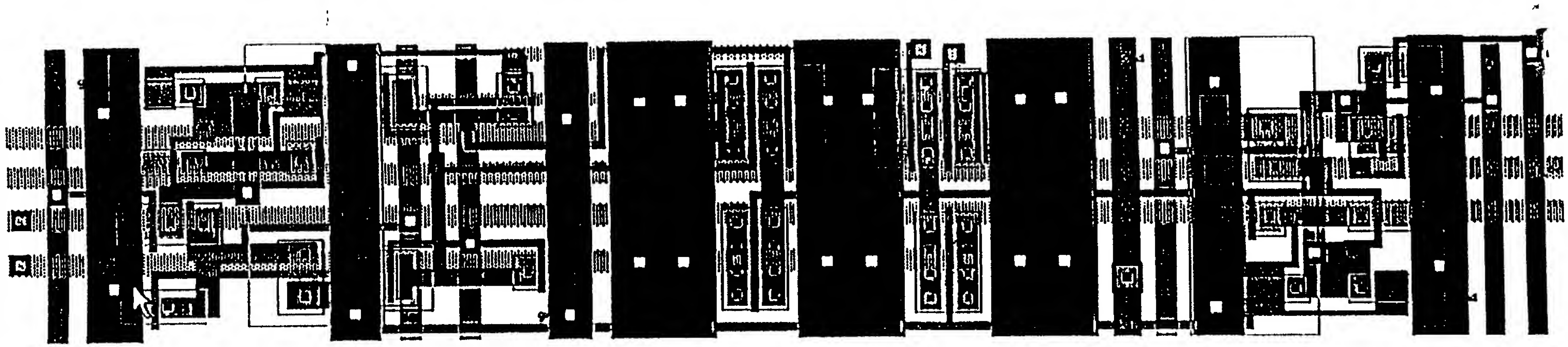

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Fig 5

00122T 5959h260

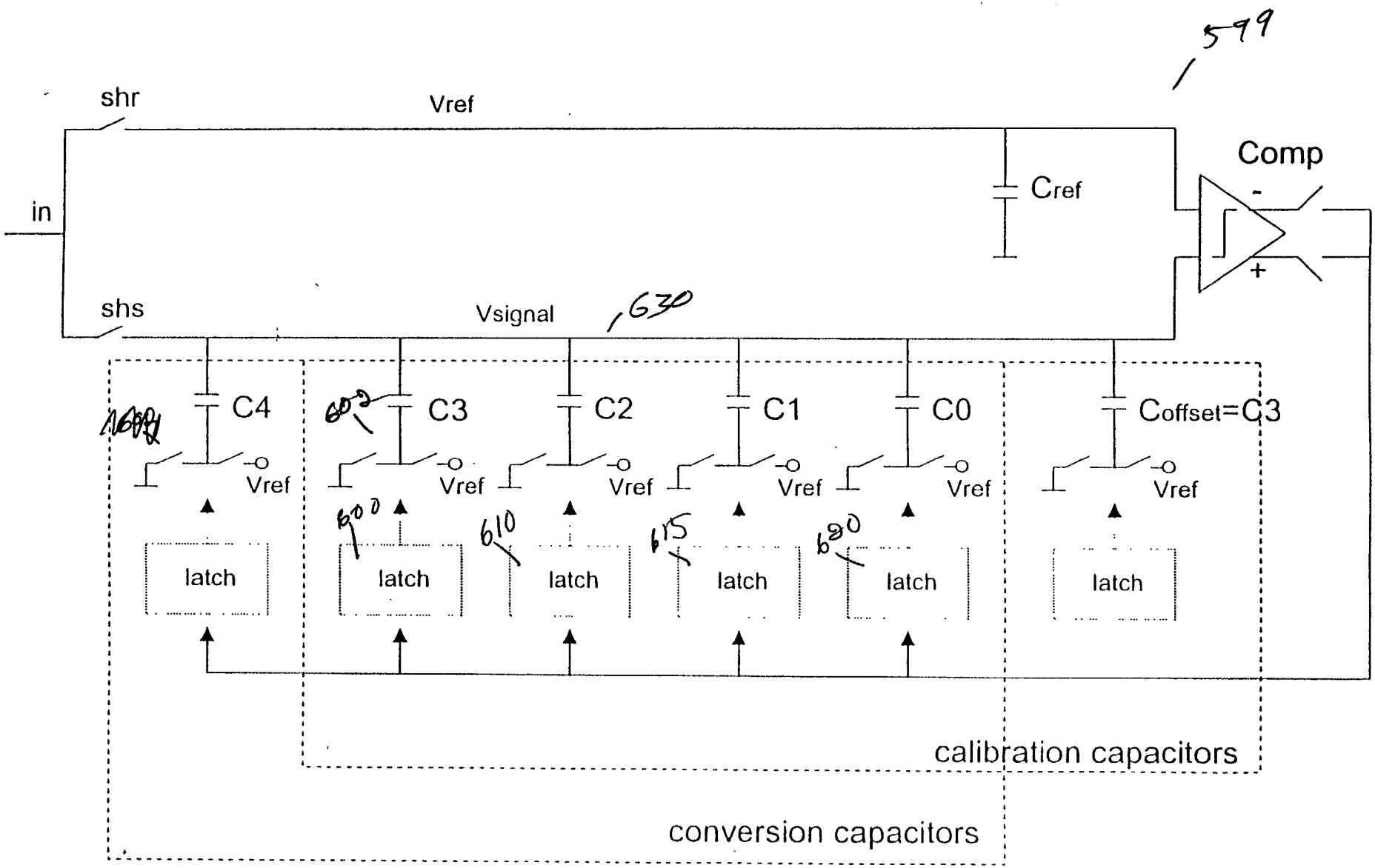

FIG 6

METHOD2.

The drawbacks of the method 1 is the need to calculate the negative value in latches. Although, the negative can be substituted with the two's complement, the error because of the substitution is 1 LSB. For better accuracy one needs either a real adder in latches, or one extra calibration smallest bit.

The method proposed here is based on a negative slope convergence during the calibration, followed by positive slope approximation during the conversion. The sketch of what the convergence process will look like is presented below

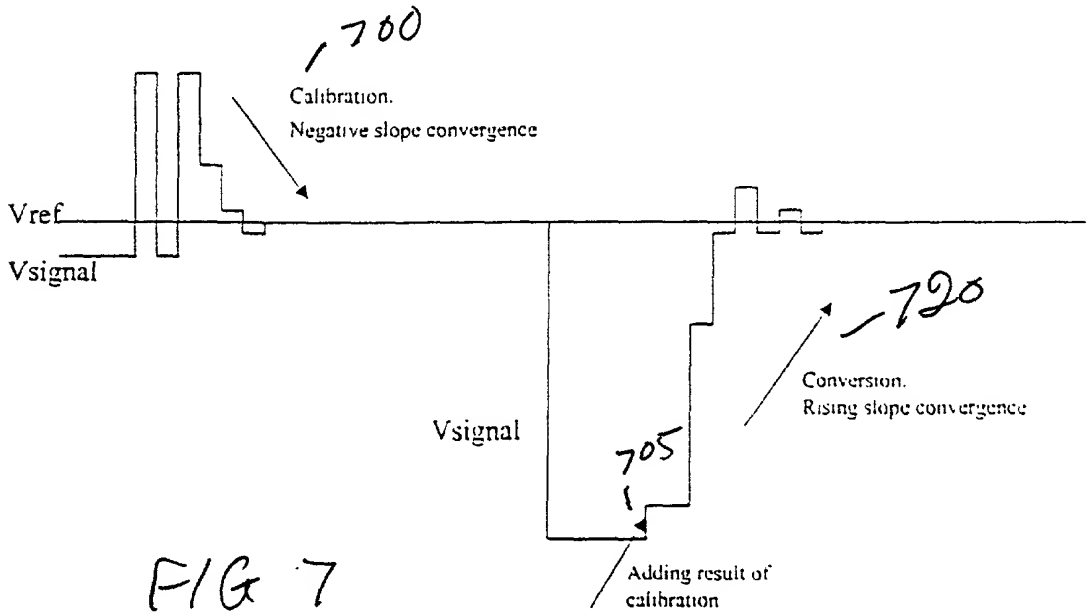

FIG 7

The ADC circuitry and example of the operation are presented in the following drawings. Note, that both comparator outputs, negative and positive are used for operation.

Sequence of operations (calibration, conversion) is the following:

- Signal for calibration is sampled while bottom plates of calibration capacitors seat at Vref. This will allow adding some negative compensation signal during calibration. But, prior to start calibration, a positive offset is added through capacitor C offset.
- During calibration, a negative compensation code is determined and stored in latches.
- To start conversion, the calibration value must be added to the signal. This is done in two steps:
  - a) for those latches which keep "0" bottom plates during signal sampling must seat at ground
  - b) for latches with "1" they must seat at Vref.

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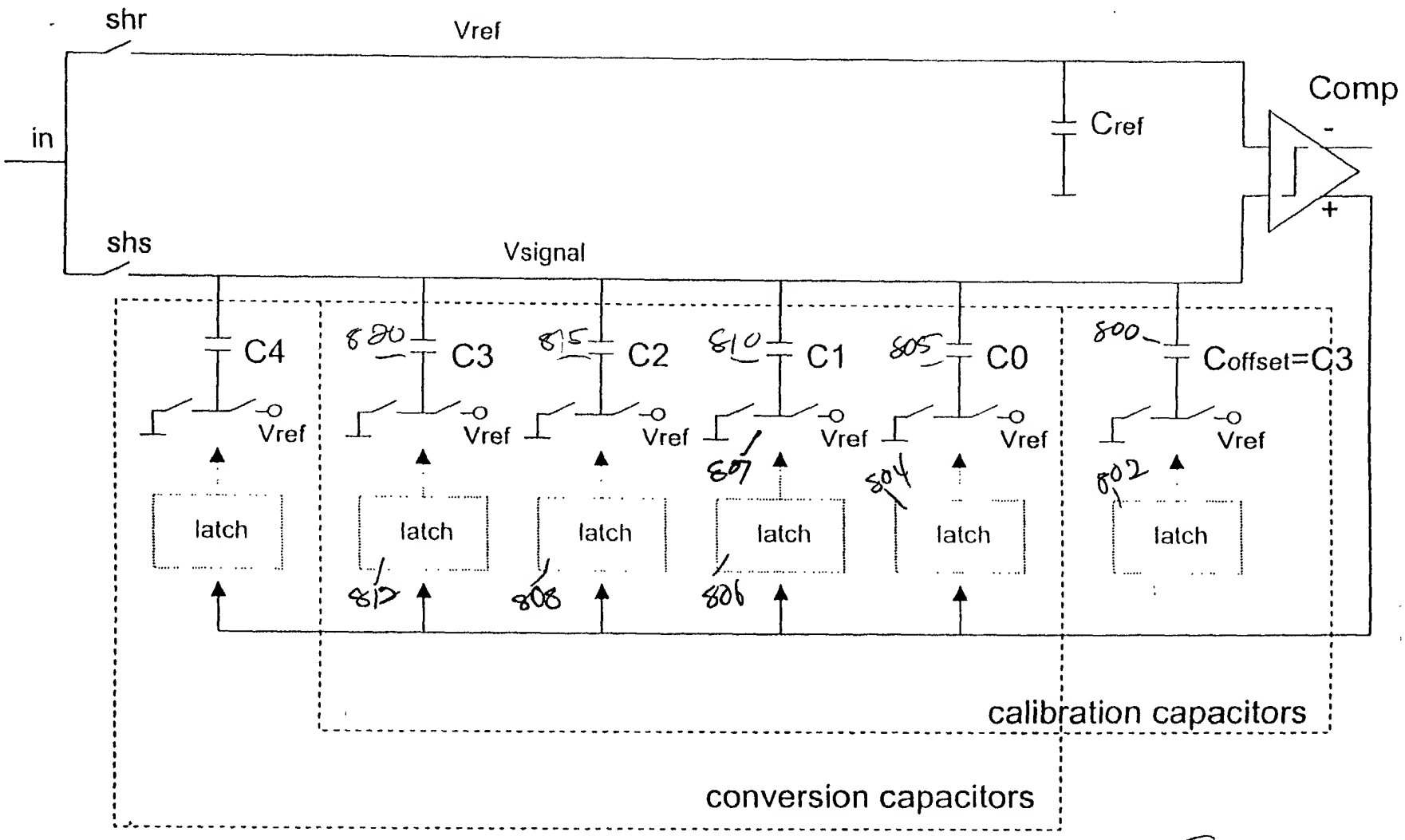

FIG 8